

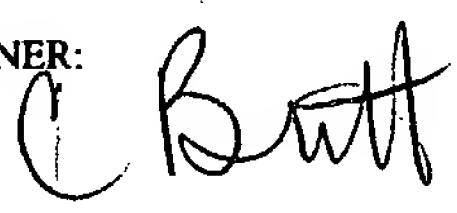
# INFORMATION DISCLOSURE STATEMENT

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  Sheet 1 of 1	Inventor(s):	B. Davies
	Title:	INTEGRATED CIRCUIT FAULT INSERTION SYSTEM
	Our Docket:	PH00-12

11000 U.S. PTO  
 09/888025  
 06/25/01

U.S. PATENT DOCUMENTS						
Examiner Initials	Cite No.	Patent Number	Kind Code	Date of Publication	Name	Relevant Passages
CB	1	5,938,779		8/17/1999	Preston	
CB	2	5,130,988		7/14/1992	Wilcox et al.	
CB	3	4,875,209		10/17/1989	Mathewes, Jr. et al.	
CB	4	4,669,081		5/26/1987	Mathewes, Jr. et al.	

OTHER PRIOR ART - NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	AUTHOR, Article Title, Publication Title, Date, Pages, Vol-Iss No, Publisher, City/Country	T
CB	1	B. Klenke, "Test Technology Overview Module 43," RASSP Program, Pennsylvania State University, 8/30/1998, Slide 85 of 173	

EXAMINER: 	DATE CONSIDERED: 5-19-04
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